In response, the Applicants would like to state that not all "photoresist techniques" are "integrated circuit photoresist techniques." For example, U.S. Patent No. 6,207,247 entitled "Method for manufacturing a molding tool used for substrate molding" shows one "photoresist technique" that is not an "integrated circuit photoresist technique", as the "master substrate contains a surface having fine pits and protuberances which may be formed by coating the substrate with a photoresist and exposing a predetermined pattern on the photoresist using a laser." (See column 5, lines 38-42.) Therefore, the Applicants respectfully request that the objection to Claim 5 kindly be withdrawn.

Rejection under 35 U.S.C. § 112, second paragraph, with respect to Claims 1-9

Claims 1-9 have been rejected under 35 U.S.C. § 112, second paragraph. The Patent Office had indicated that "In claim 1, line 3, the term "edge areas" is indefinite." The Applicants would like to point out that Figure 1 clearly shows the edge area 21 and thus the term "edge areas" is not indefinite. The Applicants would also like to state that the term "edge areas" includes not only the upper surface of the wafer but also the lower surface of the wafer, as well as the side area of the wafer connecting the upper surface and lower surface of the wafer. It should also be noted that the upper surface and the lower surface of the wafer are included in the term "edge area" only in the region of this side edge area 21. As stated earlier this also clearly follows from Figure 1, reference numeral 21. Furthermore, the Patent Office has stated that in "claim 1, lines 4-6, the phrase "the negative areas including the edge areas of the wafer" is unclear." The Applicants would like to state that "the negative areas including the edge areas of the wafer" has been clearly shown in Figure 1 as the edge area 21, which is subsequently provided with a passivation layer 27. Claim 5 has been amended in the manner suggested in the Office Action. Accordingly, withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, is hereby respectfully requested.

Rejection under 35 U.S. C. § 103 (a) with respect to Claim 1

Claim 1 has been rejected under 35 U.S.C. § 103(a). The Patent Office has contended that this claim is unpatentable over Renken et al (U.S. Patent No. 4,542,650). It is respectfully submitted that this rejection should be withdrawn for the following reasons.

In order for a claim to be rejected for obviousness under 35 U.S.C. § 103(a), not only must the prior art teach or suggest each element of the claim, the prior art must also suggest combining the elements in the manner contemplated by the claim. See Northern Telecom, Inc.

v. Datapoint Corp., 908 F. 2d 931, 934 (Fed. Cir. 1990), cert. denied 111 S.Ct. 296 (1990); In re Bond, 910 F. 2d 831, 834 (Fed. Cir. 1990). The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. See M.P.E.P. §2142. To establish a *prima facie* case of obviousness, the Examiner must show, *inter alia*, that there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references and that, when so modified or combined, the prior art teaches or suggests all of the claim limitations. See M.P.E.P. §2143. Applicant respectfully submits that neither of these criteria for obviousness are met here.

Applicants' invention in one aspect is a method of producing a micromechanical sensor arrangement, comprising the steps of: providing a wafer 20 having a surface and edge areas 21; dividing the surface of the wafer 20 into positive areas 25, 26, to be subsequently etched in a wet chemical etching process, and negative areas including the edge areas 21 of the wafer 20; providing the negative areas with a passivation layer 27 to protect the negative areas from the subsequent wet chemical etching process; etching the wafer 20 in the wet chemical etching process; and removing the passivation layer 27.

Renken on the other hand is directed to a thermal mass flow meter with a silicon substrate 60, groove 65, bridging member or web 61 and resistive pattern 62. However, this is very different than what is being disclosed and claimed by the Applicants. For example, Renken does not disclose nor does it suggest providing the edge areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process as disclosed and claimed by the Applicants. Similarly, there is no teaching and/or suggestion in Renken to divide the surface of the wafer into positive areas and negative areas, as disclosed and claimed by the Applicants. Even column 9, lines 27-28 of Renken clearly states that "layer of SiO_2 is thermally oxidized on the substrate", and thus no negative or positive areas are created. Renken in column 9, line 28 states "Photoresist is applied to all sides", and for the sake of argument, lets assume Renken's "all sides" includes "wafer edges", which would be hindsight reconstruction, and even with this assumption one would still not come up with the Applicants' invention because his "wafer edge" is not a negative area, as he had initially applied a thermal oxide layer to the entire layer, see Renken column 9, line 27, which is to be followed by the removal of the oxide layer in those areas that are to be etched later. However, according to the present invention the process is exactly reversed, that is, an exposure step is initially provided whereby areas (negative areas) are exposed on which the oxide layer is formed. And, then according to the present invention the etching process is then initiated in the other areas, i.e., the positive areas. Thus, even in Renken

the "edge areas" need to be protected by a photoresist layer, which is very delicate. In fact, Renken teaches away from Applicants' invention when he forms a continuous layer 61 and/or 61a on the bottom and top surface of the silicon substrate 60. Similarly, Renken teaches away from Applicants' invention when he forms a continuous non-reactive film/layer 67 on the surfaces adjacent the silicon substrate 60.

For the reasons discussed above, withdrawal of the rejection under 35 U.S.C. §103 (a), with respect to Claim 1 is hereby respectfully requested.

Rejection under 35 U.S. C. § 103 (a) with respect to Claims 1-3 and 5-7

Claims 1-3 and 5-7 have been rejected under 35 U.S.C. §103(a). The Patent Office has contended that these claims are unpatentable over Renken et al (U.S. Patent No. 4,542,650) in view of Pearce (U.S. Patent No. 5,711,891). It is respectfully submitted that this rejection should be withdrawn for the following reasons.

The earlier discussion with reference to Renken in connection with Claim 1 is applicable here since Claims 2, 3 and 5-7 are dependent on Claim 1. Furthermore, the criteria to be applied in obviousness rulings is also incorporated herein by reference.

Pearce teaches wafer processing using thermal nitride etch mask, however, the edge 134 that is etched back 135 is in the patterned oxide 131 and not in the substrate 111. Furthermore, Pearce does not cure the deficiencies of Renken. For example, Pearce does not disclose nor does it suggest providing the edge areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process as disclosed and claimed by the Applicants. Similarly, there is no teaching and/or suggestion in Pearce to divide the surface of the wafer into positive areas and negative areas, as disclosed and claimed by the Applicants. In fact, Pearce teaches away from Applicants' invention when he forms a continuous layer 213 and/or 215 on the surface of the silicon substrate 11. Similarly, Pearce teaches away from Applicants' invention when in column 3, lines 18-19 he teaches that "The presence of oxide layer 213 tends to seal the edges of the wafer." Even if one were to combine Renken with Pearce the resulting method would be considerably different than what has been disclosed and claimed by the Applicants. For example, one could get an invention with the substrate of Renken having sealed edges from Pearce, which is of course very different than what is disclosed and claimed by the Applicant.

Additionally, Claims 2, 3 and 5-7 are dependent on Claim 1, and as such are patentable, as Claim 1, is clearly patentable.

For the reasons discussed above, withdrawal of the rejection under 35 U.S.C. §103 (a),

with respect to Claims 1-3 and 5-7, is hereby respectfully requested.

Rejection under 35 U.S. C. § 103 (a) with respect to Claims 1-3 and 5-9

Claims 1-3 and 5-9 have been rejected under 35 U.S.C. §103(a). The Patent Office has contended that these claims are unpatentable over Iwasaki et al (U.S. Patent No. 5,804,090). It is respectfully submitted that this rejection should be withdrawn for the following reasons.

The criteria to be applied in obviousness rulings is also incorporated herein by reference.

Iwasaki discloses a process for etching semiconductors using a hydrazine and metal hydroxide-containing etching solution. Iwasaki does not disclose nor does it suggest providing the edge areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process as disclosed and claimed by the Applicants. Similarly, there is no teaching and/or suggestion in Iwasaki to divide the surface of the wafer into positive areas and negative areas, as disclosed and claimed by the Applicants. In fact, Iwasaki teaches away from Applicants' invention when in column 11, lines 36-45, he teaches that the "fabricated structure F is dipped in the etching solution 1 ... The structure F includes a silicon substrate 10 which is provided with a silicon oxide film 11 at its main surface S1 ... and a silicon oxide film 12 at its back- side surface S2 ... The back-side surface S2 serves as a surface from which the etching is initiated or starts, and therefore referred to as an etching-initiation surface", thus a layer of silicon oxide 11, 12 is first formed over the silicon substrate 10, before any further processing/etching is done on the Iwasaki substrate 10. This is similar to Renken where the oxide film is first formed over the entire wafer, and it is not the case that an oxide layer is selectively formed in exactly those areas (negative areas) which are not to be etched later, as disclosed and claimed by the Applicants. Even Figure 15A of Iwasaki has the silicon oxide film 33, 34 formed first over the "edge areas" before any etching/processing is done to the epitaxial substrate 30.

Additionally, Claims 2, 3 and 5-9 are dependent on Claim 1, and as such are patentable, as Claim 1, is clearly patentable.

For the reasons discussed above, withdrawal of the rejection under 35 U.S.C. §103 (a), with respect to Claims 1-3 and 5-9, is hereby respectfully requested.

Rejection under 35 U.S. C. § 103 (a) with respect to Claims 1-9

Claims 1-9 have been rejected under 35 U.S.C. §103(a). The Patent Office has contended that these claims are unpatentable over Iwasaki et al (U.S. Patent No. 5,804,090) in view of O'Neill (U.S. Patent No. 5,131,978). It is respectfully submitted that this rejection should be

withdrawn for the following reasons.

The earlier discussion with reference to Iwasaki in connection with Claim 1 is applicable here since Claims 2-9 are dependent on Claim 1. Furthermore, the criteria to be applied in obviousness rulings is also incorporated herein by reference.

O'Neill teaches low temperature, single side, multiple step etching process for fabrication of small and large structures, where on a planar wafer portion 10, a first masking layer 30, 30' is applied and then a second or protective layer of masking material 32, 32' is applied. After full pattern opening 12, a third masking layer 38, 38' is used to form cavity 20, channel 16, with the layers 30' and 32' covering the bottom opening of the cavity 20 until layers 30' and 32' are subsequently removed. This is very different than that which is being disclosed and claimed by the Applicants. Furthermore, O'Neill does not cure the deficiencies of Iwasaki. For example, in O'Neill there is no teaching or suggestion to divide the surface of the wafer into positive areas and negative areas prior to the wet chemical etching process, as disclosed and claimed by the Applicants. Similarly, in O'Neill there is no teaching and/or disclosure to provide the negative areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process, as disclosed and claimed by the Applicants. In fact, O'Neill teaches away from Applicants' invention when in column 4, lines 39-59, he states that on a planar wafer portion 10 "a first masking layer 30 is applied", and that "A second or protective layer of masking material 32 is formed on the silicon nitride layer masking layer 30." On the other hand, the Applicants have positive areas and negative areas defined prior to any etching. Similarly, O'Neill teaches away from Applicants' invention when in column 5, lines 14-15, he states that "The second masking layer 32 is etched with an appropriate wet etchant". Even at this "wet etching" step O'Neill still has not defined his positive and negative areas, as disclosed and claimed by the Applicants. Additionally, O'Neill teaches away from Applicants' invention when in column 5, lines 27-31, he teaches that "a third masking layer 38 ... is formed over the remaining portions of the first and second masking layers and over the exposed surfaces of the wafer formed by the opening 12." On the other hand, the Applicants are disclosing and claiming that after dividing the positive areas and the negative areas a passivation layer is provided to "protect the negative areas from the subsequent wet chemical etching process". In fact, "the positive areas 20" in O'Neill, as pointed out by the Patent Office, appear only after a portion of the third masking layer 38 is removed. Additionally, "the positive areas 20" in O'Neill, as pointed out by the Patent Office has at least one first layer 30, at least one second layer 32, and then at least one third layer 38 over it, prior to the creation of the "the positive areas 20" in O'Neill, as pointed out by the

Patent Office. Furthermore, with regard to edge protection of the wafer using Applicants' negative technique, a further difference between O'Neill and the Applicants is that even when removal of resist from the edge of the wafer is missing (which is, however, not standard in IC processing) in mass production using procedures customary up till now (and described in the art) "no silicon wafers are etched with potassium hydroxide (KOH)", without undergoing slight etching at the wafer edge. In a positive technique, the edge of the wafer has to be protected by resist which is extremely susceptible to damage. With the Applicants' method one obtains the "perfect" edge protection even with the standard semiconductor photo technique.

Additionally, Claims 2-9 are dependent on Claim 1, and as such are patentable, as Claim 1, is clearly patentable.

For the reasons discussed above, withdrawal of the rejection under 35 U.S.C. §103 (a), with respect to Claims 1-9, is hereby respectfully requested.

Conclusion

It is believed that this application is now in condition for allowance and applicants respectfully request such action.

Respectfully Submitted,

KENYON & KENYON

A212 M. Ahoan
Reg. No. 32,100

Dated: MAY 30, 2001

By: for R. L. Mayer
Richard L. Mayer
(Reg. No. 22,490)

One Broadway
New York, NY 10004
(212) 425-7200

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend Claim 5 as follows:

5. (Twice Amended) The method according to claim 2, wherein the photoresist technique used is [a standard] an integrated circuit photoresist technique.